

**ASSIGNMENT 10**

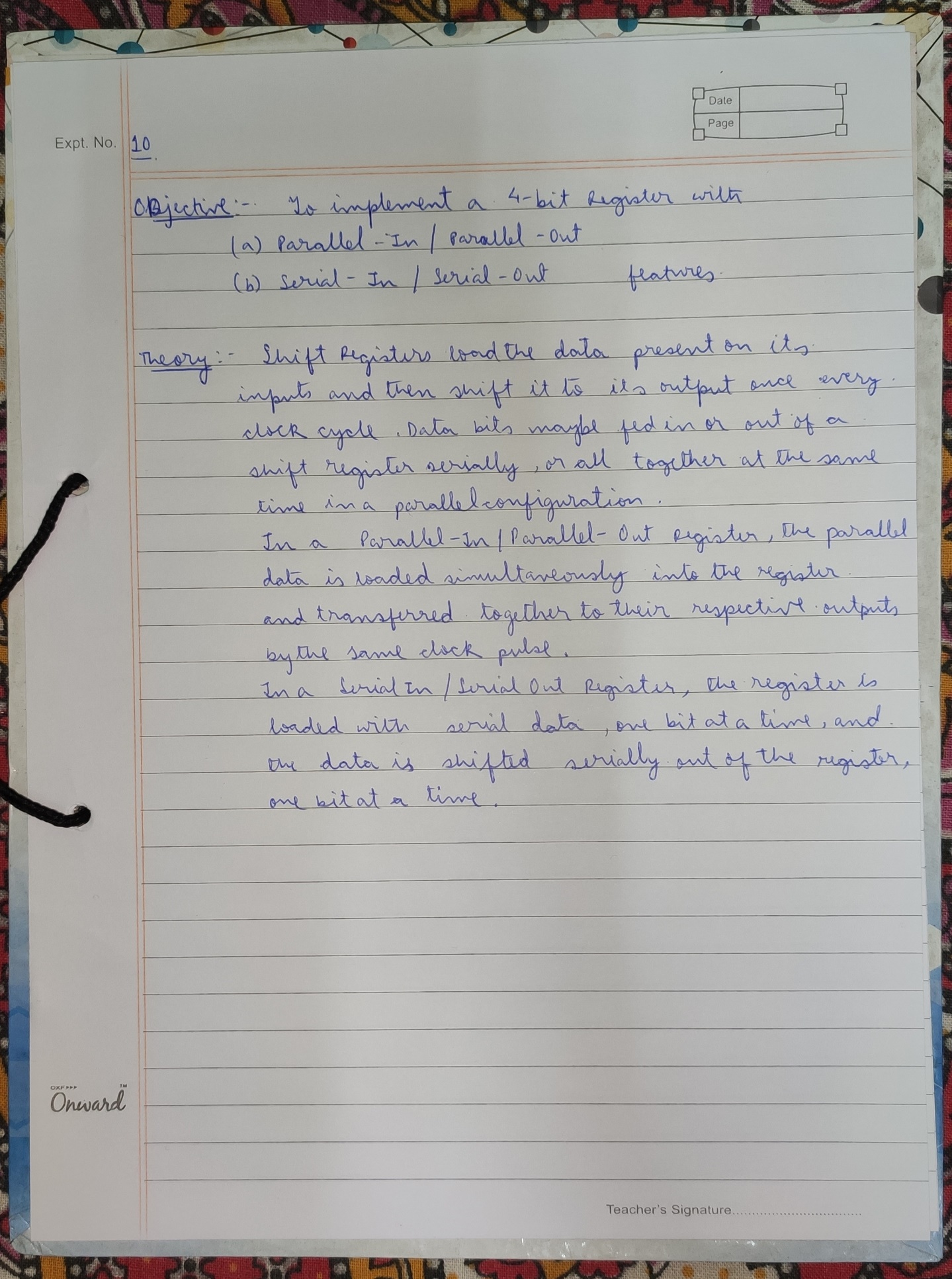
[Design a **4-BIT REGISTER** with (i) parallel-in/parallel-out (ii) serial-in/serial-out features using 2 input NAND GATES]



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**CIRCUIT DIAGRAM:**

